
SME306 Project Description

A 4x4-bit Array Multiplier

Objectives

To practice the CMOS VLSI design process through the example of a 4x4-bit array multiplier.

Introduction

The circuit you will be designing is a 4-bit array multiplier, i.e. a circuit with two 4-bit unsigned numbers as inputs, and the 8-bit product of these two numbers as the output. You will use the 0.18- μm CMOS process, the supply voltage is 1.8V, and the 8-bit bus output has to drive a 50-fF capacitive load for each bit. The objective of the project is to realize the 4x4-bit multiplier and to demonstrate its full functionality through post-layout simulation.

Background

The algorithm for a 4x4 bit multiplication is shown in Figure 1, where P_{ij} is the product (AND) of bit i of the multiplicand X (top number) with bit j of the multiplier Y , and Z_i is the sum of the column of numbers above it.

$$\begin{array}{r}
 \begin{array}{cccc}
 & X_3 & X_2 & X_1 & X_0 \\
 X & Y_3 & Y_2 & Y_1 & Y_0 \\
 \hline
 & P_{30} & P_{20} & P_{10} & P_{00} \\
 & P_{31} & P_{21} & P_{11} & P_{01} \\
 & P_{32} & P_{22} & P_{12} & P_{02} \\
 + & P_{33} & P_{23} & P_{13} & P_{03} \\
 \hline
 Z_7 & Z_6 & Z_5 & Z_4 & Z_3 & Z_2 & Z_1 & Z_0
 \end{array}
 \end{array}$$

Fig. 1 The algorithm of a 4x4-bit multiplier

Figure 2 shows an example of a 4x3-bit array multiplier in which the inputs are fed to the circuit in parallel and the outputs are also obtained in parallel after a certain delay due to the propagation of the data within the array.

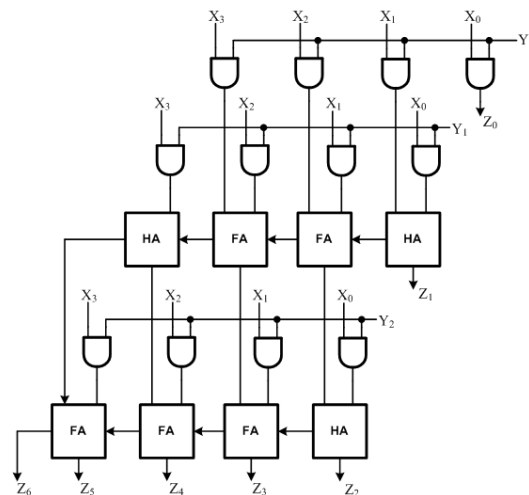


Fig. 2 The architecture of a 4x3-bit multiplier, where HA and FA stand for half-adder and full-adder, respectively

Extend the architecture of Figure 2 in order to support a 4x4-bit operation. Propose an

optimized circuit for the different blocks of the array multiplier and design it in full-custom.

Tasks to be achieved in the project

Propose a 4x4-bit array multiplier architecture. Design the circuit. Simulate the schematic level design. Draw the physical layout. Verify the design through post-layout simulation as well. Describe your work in a report where the performance is outlined (see the sample report provided on the course web site). Finally, demonstrate the operation of your design during the demonstration session.

A more detailed description of the tasks:

1. Circuit architecture and design: Describe the architecture and the VLSI design of the CMOS transistor circuit for the design. You must use **static CMOS design with minimum number of transistors and optimized delay and silicon area**. The supply voltage is 1.8 V and each output has to drive a 50-fF capacitive load. The two 4-bit unsigned input numbers X & Y must be named as **X0 to X3** (X0 is LSB) and **Y0 to Y3** (Y0 is LSB), respectively. Moreover, the 8-bit output must be named as **Z0 to Z7** (Z0 is LSB). **(Note: You MUST strictly follow the pin names stated here otherwise your mark will be deducted)**.
2. Functional simulation: Show the proper functionality of the final circuit as well as all the building blocks. Analyze the critical path delay and show the floor-planning used in order to optimize the silicon area. Your floor-plan should also show the distribution of all the signals and the power supply.
3. Layout: Design an optimized layout in terms of area and parasitic capacitance (reduced diffusion capacitance of critical nodes and optimized routing). Describe how your layout was optimized and show the results of your LVS verifications.
4. Post-Layout Simulation: use the post-layout simulation to verify the functionality of your circuit and also to extract the final performance that should be included in your final report. Performance would include: delay and silicon area.
5. Report: Refer to the sample report on the course web site for more explanations on the format of the report and content.

Grading

This project is worth **40%** of the total course mark. The project grading scheme is as follows. **15%** is allocated to the **report**. **15%** is allocated to the **functionality** of the final circuit, in which **7.5%** is for the functionality of the schematic and **7.5%** for the layout. If your design is completed and functions properly both in the schematic and the layout levels, then **10%** is allocated to the **performance** in terms of layout area and layout delay of the design. However, if your design fails to function or is not completed in schematic and/or layout levels, you will get zero mark on functionality and performance.

Project Group

Partners: You are asked to **form a group of 2 students**. You must make sure that the instructor and/or TA are informed of your group by **16 Apr. 2021 (Fri., week 9)**. No change of partner is allowed after that date. Note: You may do the project by yourself (i.e., 1 student as a group), but you also need to inform the TA before the same due date.

1. Project demonstrations: The project demonstrations will be on **27 May 2021 (8AM to 12:10PM, Thu., week 15) (for class 1) and 28 May 2021 (2PM to 6:10PM, Fri., week 15) (for class 2)**. All group members are required to be present during the project demonstration. During the project demonstration, a certain number of input vectors (same for all groups) will be applied to the circuits to verify the functionality. The input vectors that will be applied to the circuits to verify the functionality will not be released prior to the demonstration. The longest delay (propagation delay) will be measured and recorded. A performance metric will be calculated: $\text{performance} = 1 / [\text{delay} * \text{area}]$. The higher the performance is, the better the grade will be. The performance values for all the groups will be ranked and graded.

3. Workload: The work of the project should be done by all members of the group. You are responsible for the distribution of the tasks and the time management. **All group members are required to sign a declaration indicating the individual tasks and the relative amount of work (in %) each member of the group has contributed.**